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CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper and the documents and/or fees referred to as attached therein are being deposited with the United States Postal Service on July 6, 2000 in an envelope as "Express Mail Post Office to Addressee" service under 37 CFR § 1.10, Mailing Label Number **EL563119243US**, addressed to the Assistant Commissioner for Patents, Washington, DC 20231.

Rick von Wohld

Attorney Docket No. LAM1P077A

First Named Inventor: Andras Kuthi

UTILITY PATENT APPLICATION TRANSMITTAL (37 CFR. § 1.53(b))
(Continuation, Divisional or Continuation-in-part application)

Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

☐ Duplicate for fee processing

Sir: This is a request for filing a patent application under 37 CFR. § 1.53(b) in the name of inventor:
Andras Kuthi and Lumin Li

For: **METHOD FOR MAKING A SEMICONDUCTOR PROCESS CHAMBER ELECTRODE (As Amended)**

This application is a ☐ Continuation ☒ Divisional ☐ Continuation-in-part of prior Application No. **09/100,268**, from which priority under 35 U.S.C. § 120 is claimed.

Application Elements:

☒ 28 Pages of Specification, Claims and Abstract
☒ 09 Sheets of informal Drawings
☒ Combined Declaration and Power of Attorney
☐ Newly executed (original or copy)
☒ Copy from a prior application (37 CFR 1.63(d) for a continuation or divisional). The entire disclosure of the prior application from which a copy of the declaration is herein supplied is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
☐ Deletion of inventors Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

Accompanying Application Parts:

☐ Assignment and Assignment Recordation Cover Sheet (recording fee of $40.00 enclosed)
☐ Power of Attorney
☐ 37 CFR 3.73(b) Statement by Assignee

☐ Information Disclosure Statement with Form PTO-1449 ☐ Copies of IDS Citations

☒ Preliminary Amendment (*New claims numbered after highest original claim in prior application.*)

☒ Return Receipt Postcard

☐ Small Entity Statement(s) ☐ Statement filed in prior application. Status still proper and desired.

☒ Other: Change of Attorney's Address

Claim For Foreign Priority

☐ Priority of _____ Application No. _____ filed on _____ is claimed under 35 U.S.C. § 119.

☐ The certified copy has been filed in prior application U.S. Application No. _____

☐ The certified copy will follow.

Extension of Time for Prior Pending Application

☐ A Petition for Extension of Time is being concurrently filed in the prior pending application. A copy of the Petition for Extension of Time is attached.

Assignment

☒ The prior application is assigned of record to Lam Research Corporation.

Amendments

☒ Amend the specification by inserting before the first line the sentence: "This is a

☐ Continuation ☐ Continuation-in-part ☒ Divisional application of copending prior

☒ Application No. 09/100,268 filed on June 19, 1998,

☐ International Application _____filed on _____ which designated the United States,

the disclosure of which is incorporated herein by reference."

☐ Cancel in this application original claims _____ of the prior application before calculating the filing fee. (*At least one original independent claim must be retained.*)

Fee Calculation (37 CFR § 1.16)

	(Col. 1) NO. FILED	(Col. 2) NO. EXTRA	SMALL ENTITY RATE	FEE	OR	LARGE ENTITY RATE	FEE
BASIC FEE			$345	$	OR	$690	$690.00
TOTAL CLAIMS	08	-20 = 0	x09 =	$	OR	x18 =	$
INDEP CLAIMS	01	-03 = 0	x39 =	$	OR	x78 =	$
[ ] Multiple Dependent Claim Presented			$130 =	$	OR	$260 =	$
* If the difference in Col. 1 is less than zero, enter "0" in Col. 2.			Total	$	OR	Total	$690.00

☒ Check No. 4012 in the amount of $690.00 is enclosed.

☒ The Commissioner is authorized to charge any fees beyond the amount enclosed which may be required, or to credit any overpayment, to Deposit Account No. 50-0805 (Order No. LAM1P077A).

General Authorization for Petition for Extension of Time (37 CFR § 1.136)

☒ Applicant hereby makes and generally authorizes any Petitions for Extensions of Time as may be needed for any subsequent filings. The Commissioner is also authorized to charge any extension fees under 37 CFR § 1.17 as may be needed to Deposit Account No. 50-0805 (LAM1P077A).

☒ Please send correspondence to the following address (*please do not send correspondence to the address cited in the copy of the declaration being filed herewith*):

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Date: July 6, 2000

Albert S. Penilla, Esq.
Registration No. **39,487**

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	)	Docket No: LAM1P077A
Kuthi, et al.	)	Group Art Unit: Unknown
Application No: Unknown	)	Examiner: Unknown
Filed: July 6, 2000	)	
For: METHOD FOR MAKING A SEMICONDUCTOR PROCESS CHAMBER ELECTRODE (As amended)	)	July 6, 2000

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper and the documents and/or fees referred to as attached therein are being deposited with the United States Postal Service on July 6, 2000 in an envelope as "Express Mail Post Office to Addressee" service under 37 CFR § 1.10, Mailing Label Number **EL563119243US**, addressed to the Assistant Commissioner for Patents, Washington, DC 20231.

Rick von Wohld

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The following is a preliminary amendment amending the specification and claims. Please enter the following amendments and remarks:

IN THE TITLE

Please amend the title as follows:

Please change the title from "Semiconductor Process Chamber Electrode and Method for Making the Same" to --Method for Making a Semiconductor Process Chamber Electrode--.

IN THE SPECIFICATION

Page 13, line 23, please delete "5 mm," and replace with "0.5 mm,".

IN THE CLAIMS

All claims pending after this amendment are listed below. Please amend the claims as follows:

Please cancel claims 1-13 and 22-32.

14. (Amended) In a chamber for processing a semiconductor wafer through plasma etching operations, the chamber including a support chuck for holding the semiconductor wafer and a pair of RF power sources; a method for making a top electrode for the chamber, comprising:

forming the top electrode to have a center region, a first surface and a second surface, the first surface has an inlet that is configured to receive processing gases from a source that is external to the system and flow the processing gases into the center region, the second surface has a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings are configured to define the second surface which is located [an electrode surface that is defined] over a wafer surface of the semiconductor wafer.

15. The method for making a top electrode for the chamber as recited in claim 14, further comprising:

coupling the top electrode to one of the pair of RF power sources and the support chuck to the other one of the pair of RF power sources.

16. (Amended) The method for making a top electrode for the chamber as recited in claim 15, further comprising:

forming the electrode openings to be at least about [5] 0.5 mm or greater in diameter and the gas feed holes to have a diameter of about [1] 0.1 mm.

17. The method for making a top electrode for the chamber as recited in claim 15, further comprising:

defining the electrode openings to a depth of between about 1/32 inch and ¼ inch.

18. The method for making a top electrode for the chamber as recited in claim 16, further comprising:

fixing a separation of between about 0.75 cm and about 4 cm between the electrode surface and the wafer surface.

19. The method for making a top electrode for the chamber as recited in claim 18, further comprising:

inserting two or more gas buffer plates within the center region of the top electrode.

20. The method for making a top electrode for the chamber as recited in claim 18, further comprising:

striking a plasma between the separation, the plasma having a first plasma sheath that is proximate to the wafer surface and a second plasma sheath that outlines an inner region of the top electrode openings, such that the second plasma sheath has an area that is greater than the first plasma sheath.

21. The method for making a top electrode for the chamber as recited in claim 20, further comprising:

increasing an ion bombardment energy over the wafer surface when the second plasma sheath has the area that is greater than the first plasma sheath.

REMARKS

Claims 14-21 are pending after entry of this preliminary amendment. Claims 1-13 and 22-32 have been canceled.

The Specification has been amended to correct an error on line 23 of page 13, and is now consistent with the dimensions described on line 4 of the same page.

This preliminary amendment is filed with a divisional of Application Number 09/100,268, filed on June 19, 1998. This divisional is being filed under 37 C.F.R. §1.53(b), in response to a restriction requirement under 35 U.S.C. § 121. All claims are therefore drawn to the invention of Group II, as designated by the Examiner in telephone conference on November 2, 1999, and in an Office Action dated November 26, 1999.

It is believed that the claims, in their present form, are in a condition for allowance. As such, a notice of allowance is respectfully requested. If the Examiner has any questions concerning the present response, the Examiner is kindly requested to contact the undersigned

at (408) 749-6900. If any additional fees are due in connection with filing this response, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM1P077A). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
MARTINE PENILLA & KIM, LLP

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ATTORNEY DOCKET No.
P0393/LAM1P077

PATENT APPLICATION

SEMICONDUCTOR PROCESS CHAMBER ELECTRODE AND METHOD FOR MAKING THE SAME

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SEMICONDUCTOR PROCESS CHAMBER ELECTRODE AND METHOD FOR MAKING THE SAME

By Inventors
Andras Kuthi
Lumin Li

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to semiconductor fabrication equipment, and more particularly, the present invention relates to improved semiconductor processing chamber electrodes and methods for making and implementing the improved electrodes.

2. Description of the Related Art

In semiconductor fabrication, integrated circuit devices are fabricated from semiconductor wafers that are placed through numerous processing operations. Many of the numerous processing operations are commonly carried out in processing chambers in which layers, such as, dielectric and metallization materials are successively applied and patterned to form multi-layered structures. For example, some of these layers (*e.g.*, SiO_2) are commonly deposited in chemical vapor deposition (CVD) chambers, and then photoresist materials are spin-coated and placed through photolithography patterning. When a photoresist mask is defined over a particular surface, the semiconductor wafer is placed into a plasma etching chamber in order to remove (i.e., etch) portions of the underlying materials that are not covered by the photoresist mask.

Figure 1A shows a semiconductor processing system 100 including a chamber 102 that is used for processing semiconductor wafers through etching operations. In

this example, the chamber 102 includes a chuck 104 which is configured to support a semiconductor wafer 106. The chuck 104 also supports a plurality of quartz rings 108. Over a topmost quartz ring 108, sits a ceramic ring holder 110, which is configured to hold a top electrode 114. The top electrode 114 is configured to receive processing gases which will be distributed into the plasma region 112 during processing.

The top electrode is also shown coupled to a match box and diplexer 116a and an RF power source 118a. The chuck 104 is also coupled to a match box and diplexer 116b and an RF power source 118b. The chamber 102 is provided with outlets 120 which are configured to pump out excess gases from within the chamber during processing. In operation, the RF power supply 118a is configured to bias the top electrode 114 and operate at frequencies of about 27 MHz. The RF power source 118a is primarily responsible for generating most of the plasma density within the plasma region 112, while the RF power source 118b is primarily responsible for generating a bias voltage within the plasma region 112. The RF power source 118b generally operates at lower frequencies in the range of about 2 MHz.

Figure 1B provides a more detailed view of the top electrode 114 of the semiconductor processing system 100. The top electrode 114 generally includes a number of gas buffer plates 122 which have a plurality of holes defined throughout their surface region, and are configured to evenly distribute the processing gases throughout the top electrode 114. In this manner, the gas buffer plates 112 will ensure that an about equal amount of gas is allowed to flow out of each of the gas feed holes 128 of a silicon plate 126. The top electrode 114 also has a graphite ring 124 which is configured to mount onto the ceramic holders 110 of Figure 1A. Once

the process gases are allowed to flow out of the gas feed holes 128, a plasma may be generated in the plasma region 112 that is defined between the surface of the silicon plate 126 and a surface of the wafer 106.

During operation, the RF power 118a and the RF power 118b is applied to the top electrode 114 and the chuck 104, respectively. Once the process gases are channeled into the top electrode 114 and allowed to flow out of the gas feed holes 128 into the plasma region 112, a plasma sheath 131 and 132 will be defined within the plasma region 112 as shown in Figure 1C.

As pictorially shown, the silicon plate 126 will have an electrode surface 134 which is directly opposite a wafer surface 136 of the semiconductor wafer 106. As is well understood in plasma physics, the electrode surface 134 and the wafer surface 136 are partially responsible for producing the plasma sheaths 131 and 132 within the plasma region 112.

Specifically, as shown in Figure 1D, plasma sheaths edges are defined at points 133a and 133b along a plasma density profile 133. The plasma density profile illustrates that the plasma concentration falls to about zero near the wafer surface 136 and the top electrode surface 134. As such, the plasma concentration gradually increases from zero up to a constant concentration between points 133a and 133b. The electrode surface 134 and the wafer surface 136 will therefore ensure that the bulk of the plasma is contained between the plasma sheaths 131 and 132 as shown in Figure 1C.

As the demand to etch smaller and smaller integrated circuit device patterns continues to increase, more difficult high aspect ratio etching will be needed. As

shown in Figure 1E, a cross sectional view 140 of a wafer substrate 106' is shown. The wafer substrate 106' has a dielectric layer 140 deposited thereon and a patterned photoresist layer 142. The photoresist layer 142 has a patterned window 144 defining a window down to the dielectric layer 140. As the aspect ratios continue to increase (*i.e.*, deeper and narrower etching geometries), a process window that defines a set of controllable process parameters will also rapidly shrink. When the process window shrinks, adjustment of process parameters will no longer improve etch rates, etch selectivities, or etch profiles.

Typically, the process parameters include pressure settings, flow rates, electrode biasing powers, types of processing chemistries, and so on. However, as aspect ratios continue to increase, varying the process window parameters no longer assist a processing chamber's ability to control a desired etching operation. For example, when a geometry such as that defined by the patterned window 144 (i.e., for a contact via or the like) in the photoresist layer 142 is desired, the best etching chemistries may no longer be able to etch all the way down through the dielectric layer 140. When that happens, a premature etch stop 146 will develop because the processing chemistries will also be depositing polymers on the sidewalls and the bottom during the etching operation. As is well known, this polymer deposition can seriously retard the etching of dielectric layers 140 when high aspect ratio patterns are the subject of etching.

In efforts to combat this problem, process engineers have in the past, attempted to increase the level of oxygen within the processing chamber during an etch operation. Unfortunately, when the oxygen level is increased within the processing chamber, the etching operation will produce a bow-shaped etch 148 within

the dielectric layer 140. As can be appreciated, when such a bow-shaped etch 148 occur within the dielectric layer 140, subsequent filling of the via hole defined by the bow-shaped etch 148 will be problematic. That is, conventional conductive fill techniques used to deposit metallization within a via hole may not work because of the bow-shaped etch via 148. As a result, a fabricated device having the bow-shaped etch via holes 148 may fail to function within its intended design.

Another solution attempted in the prior art has been to increase the bias power of the RF power source 118b that is coupled to the chuck 104 in an attempt to increase the ion bombardment energy over the surface of the wafer 106. However, when the bias voltage of the RF power source 118b is increased, more plasma is also generated within the plasma region 114, which counteracts the increase in ion bombardment energy. In addition, the processing molecules channeled into the plasma region 112 may change their chemical composition when the bias power is increased, and therefore, may fail to perform the desired etching. Consequently, it has been observed that merely increasing the RF power that is applied to the chuck 104 does not help in improving the etching of high aspect ratio geometries.

In view of the foregoing, what is needed is a processing apparatus and method for making and implementing the apparatus which will assist in increasing the ion bombardment energy at the surface of a wafer without also increasing the plasma density or changing the chemical composition of the processing molecules.

SUMMARY OF THE INVENTION

The present invention fills these needs by providing a semiconductor processing chamber electrode that assists in shifting an increased ion bombardment energy toward the surface of the semiconductor wafer. It should be appreciated that the present invention can be implemented in numerous ways, including as a process, an apparatus, a system, a device, and a method. Several inventive embodiments of the present invention are described below.

In one embodiment, a system for processing a semiconductor wafer through plasma etching operations is disclosed. The system has a process chamber that includes a support chuck for holding the semiconductor wafer and a pair of RF power sources. The system further includes an electrode that is positioned within the system and over the semiconductor wafer. The electrode has a center region, a first surface and a second surface. The first surface is configured to receive processing gases from a source that is external to the system and flow the processing gases into the center region. The second surface has a plurality of gas feed holes that are continuously coupled to a corresponding plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes. The plurality of electrode openings are configured to define an electrode surface that is defined over a wafer surface of the semiconductor wafer. The electrode surface assists in increasing an electrode plasma sheath area in order to cause a shift in bias voltage onto the wafer surface, thereby increasing the ion bombardment energy over the wafer without increasing the plasma density.

In another embodiment, a method for making a top electrode that is positioned in a chamber for processing a semiconductor wafer through plasma etching operations is disclosed. The chamber includes a support chuck for holding the semiconductor wafer and a pair of RF power sources. The method includes forming the top electrode to have a center region, a first surface and a second surface. The first surface has an inlet that is configured to receive processing gases from a source that is external to the system and flow the processing gases into the center region. The second surface has a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes. The plurality of electrode openings are configured to define an electrode surface that is defined over a wafer surface of the semiconductor wafer.

In yet another embodiment, a plasma process chamber for processing a semiconductor wafer is disclosed. The plasma process chamber includes a support chuck for holding the semiconductor wafer and a pair of RF power sources. The plasma process chamber includes an electrode means for providing gas chemistries into a process region that is defined between the electrode means and a wafer surface of the semiconductor wafer. The electrode means has a plurality of oversized gas feed holes that are configured to define an electrode surface over the wafer surface. When a plasma is generated between the electrode surface and the wafer surface in the plasma process chamber, a substantially planar first plasma sheath is defined over the wafer surface and a contoured second plasma sheath is defined over the electrode surface. The contoured second plasma sheath is configured to extend into the plurality of oversized gas feed holes, and therefore the contoured second plasma

sheath has a greater surface area than the substantially planar first plasma sheath. The greater surface area therefore causes an increased bias voltage over the wafer surface and a decreased bias voltage over the electrode surface.

Advantageously, it is now possible to increase the bias voltage over the surface of the wafer without also causing an increase in plasma density. Because an increased bias voltage is essentially an increase in ion bombardment energy, higher aspect ratio geometries can now be etched without causing premature etch stops or bow etch profiles. These and other advantages of the present invention will become apparent upon reading the following detailed descriptions and studying the various figures of the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention, together with further advantages thereof, may best be understood by reference to the following description taken in conjunction with the accompanying drawings.

Figure 1A shows a semiconductor processing system including a chamber that is used for processing semiconductor wafers through etching operations.

Figure 1B provides a more detailed view of a top electrode of a semiconductor processing system.

Figure 1C shows a plasma and plasma sheaths formed next to an electrode surface and a wafer surface.

Figure 1D shows a plasma concentration profile and the plasma sheath locations relative to an electrode surface and a wafer surface.

Figure 1E shows a cross sectional view of a semiconductor substrate undergoing an etch operation.

Figure 2A shows a cross sectional view of a top electrode in accordance with one embodiment of the present invention.

Figure 2B shows a plan view of a surface of the electrode body in accordance with one embodiment of the present invention.

Figure 2C shows a more detailed view of the electrode opening of Figure 2A in accordance with one embodiment of the present invention.

Figure 2D shows an alternative detailed view of an electrode opening in accordance with one embodiment of the present invention.

Figure 2E shows a more detailed view of the electrode opening surfaces, a wafer surface, and a corresponding plasma having plasma sheaths in accordance with one embodiment of the present invention.

Figure 3 shows a more detailed view of a contoured plasma sheath that is defined into the electrode openings and a substantially planar plasma sheath that is defined over the wafer surface in accordance with one embodiment of the present invention.

Figure 4A shows voltage waveforms plotted over time, including a shifted voltage waveform that causes a shift in bias voltage in accordance with one embodiment of the present invention.

Figure 4B shows a graph illustrating the resulting current magnitudes over a cycle of a shifted voltage waveform of Figure 4A in accordance with one embodiment of the present invention.

Figure 5 is a graph illustrating bias vs. area ratio for the plasma sheaths of a top electrode and a wafer in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

An invention is described for a semiconductor processing chamber electrode that assists in shifting an increased plasma ion bombardment energy toward the surface of the semiconductor wafer to improve etching of high aspect ratio geometries. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be obvious, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process steps have not been described in detail in order not to unnecessarily obscure the present invention.

As described above, the present invention discloses a unique top electrode that enables processing chambers to retain control of processing windows during high aspect ratio etching operations. Although the top electrodes of the present invention can be implemented into many different types of processing chambers, one exemplary chamber that will benefit from the inventive design features of the disclosed top electrodes is a Lam Research Rainbow 4520XL processing chamber, which is available from Lam Research Corporation of Fremont, California. In some chamber orientations, the top electrode may be grounded and both frequencies are fed to the bottom electrode (i.e., wafer support chuck). In either case, the top electrode configuration of the present invention will assist in increasing the ion bombardment energy on the surface of the wafer without the side effects of the prior art.

Figure 2A shows a cross sectional view of a top electrode 200 in accordance with one embodiment of the present invention. In this embodiment, the top electrode

200 includes an electrode body 202 that has a plurality of electrode regions 202c that define respective electrode openings 202b. The electrode openings 202b form a channel that leads to a plurality of gas feed holes 228. In general, the gas feed holes 228 channel the processing gases to a plasma region 112, as described with respect to Figure 1A. Accordingly, when the top electrode 200 is inserted into a semiconductor processing system chamber, a surface 234 of the electrode body 202 will define the surface that is in close proximity to a generated plasma sheath.

In a preferred embodiment of the present invention, the inter-portion of the electrode body 202 will preferably have an opening 250 which is about the same diameter of a wafer being processed. For example, when an 8-inch wafer is being processed, the diameter 250 is preferably sized to be about 8 inches. Although not shown, gas buffer plates are typically positioned within the electrode body 202. The electrode body 202 has a preferred thickness 252 of about 1 inch, while the electrode regions 202c have a thickness 256 that is about ¼ inch. Of course, these exemplary dimensions may be modified depending on the size of the semiconductor wafer being processed.

Figure 2B shows a plan view of the surface 234 of the electrode body 202 in accordance with one embodiment of the present invention. As shown, the electrode openings 202b are preferably arranged throughout the surface 234 in a hexagonal pattern arrangement. In this hexagonal pattern arrangement, the separation 203 between the electrode openings 202b is preferably set to about 0.375 inches. Also, in a preferred embodiment, the diameter of each of the electrode openings 202b is set to be about 0.25 inches.

Figure 2C shows a more detailed view of the electrode opening 202b of Figure 2A in accordance with one embodiment of the present invention. The electrode opening 202b has a diameter D_3 242 that is selected to be at least equal to or greater than about 5 Λ_{Debye} (*i.e.*, $\geq$ 0.5 mm). The depth D_4 244 of the electrode opening 202b is preferably set to be between about 1/32 inch and about ¼ inch, and more preferably between about 1/16 inch and about ¼ inch, and most preferably about 1/8 inch. Preferably, the diameter D_2 240 is about 0.1 mm. In this embodiment, the electrode opening 202b has an angled (about 30 degrees) surface 246, which is caused by the profile of a machining drill bit. However, it should be understood that other angles will work as well. For example, Figure 2D shows a case in which the angled surface 246 is replaced with a right angle 248. Of course, when the angled surface 246 is removed, the electrode opening 202b may extend to a distance D_5 249, which may be greater than distance D_4 244.

Figure 2E shows a cross sectional view of three electrode regions 202c and a cross section of the wafer 206 in accordance with one embodiment of the present invention. In a preferred embodiment, the distance between the surface 234 and the wafer surface 236 is preferably set to be between about 0.75 cm and about 4 cm, and more preferably between about 1 cm and about 3 cm, and most preferably about 2 cm. Once the semiconductor processing system is placed into its operational state (*i.e.*, processing gases have been flown into the chamber, biasing powers have been set, pressures and temperatures adjusted, etc.), a plasma is generated within a plasma region 212. Because the electrode openings 202b have been increased to be at least equal to or greater than about 5 mm, a plasma sheath 231 is caused to shift into the electrode openings 202b.

As pictorially shown, the shifted plasma sheath 231 follows the profile of the electrode opening 202b walls. That is, the plasma sheath 231 is separated from the surface 234 and electrode opening surfaces 204 by a distance D_1 233. In one embodiment, the distance D_1 233 may be between about 0.5 mm, and about 5 mm, and most preferably about 2 mm. Because the plasma sheath next to the top electrode in prior art designs is not shifted as shown in Figure 1C, the surface area of both plasma sheaths will be about equal. However, because the plasma sheath 231 is shifted into the electrode openings 202b throughout the top electrode 200, the surface area of the plasma sheath 231 will be greater than the surface area of the plasma sheath 232.

Figure 3 shows a cross sectional view of the plasma sheath 231 that conforms to the surfaces of the electrode regions 202c as shown in Figure 2E, and the plasma sheath 232 that is defined above the wafer 206. Although only a cross sectional view of the sheaths 231 and 232 are shown, it should be understood that the sheaths are actually three-dimensional (3D) blankets that are defined over each of the surfaces of the top electrode 200 and the wafer 206. As such, a substantial increase in sheath $area_1$ is produced when the sheath 231 shifts into the electrode openings 202b. Table A below shows an exemplary calculation of the increase in sheath 231 surface $area_1$ compared to the sheath 232 surface $area_2$. Of course, other area increases may be obtained depending on the specific electrode opening geometries.

TABLE A TOP ELECTRODE AREA INCREASE	
Electrode Opening 202b	diameter (d = 1/4 in) depth (h = 1/8 in)
Distance Between Electrode Openings	D= 3/8 in
Transparency	$T = (d^2\pi/D^2\sqrt{3})$ T = 0.806
Added Area	$A = (d\pi h) + ((1/\cos(30 \text{ deg}))-1)d^2\pi/4$ A=0.682 cm^2
Base Area	$B = ((D^2\sqrt{3})/4)$ B = 0.393 cm^2
Area Increase	I = (B+A)/B I = 2.7

As shown from the calculations of Table A, the surface area $_1$ of the plasma sheath 231 has increased to about 2.7 times the area$_2$ of the sheath 232 that is defined over the wafer 206. In other preferred embodiments, the increase in area can be between about 1.5 and 3.5, and most preferably between about 2 and about 3.

Figure 4A shows a graph 300 depicting sinusoidal RF voltage waveforms over time in accordance with one embodiment of the present invention. In this example, a sinusoidal voltage wave 302 of a prior art design having equal area sheaths (i.e., area $_1$ = area $_2$) is shown. When the area sheaths are equal, the sinusoidal voltage wave 302 will be positive for an equal amount of time as it is negative. However, once the electrode 200 is placed into the processing chamber, the area $_1$ of the sheath 231 will

increase as shown in Figure 3. At this point, the magnitude of current (ion and electron current) flowing through the plasma will be different during the time that a current I_1 flows away from the wafer 206 in the direction of the top electrode 200 and during the time that a current I_2 flows away from the top electrode 200 in the direction of the wafer 206. In fact, because there is a greater sheath surface area$_1$ close to the top electrode surface 234/204, the current I_1 will have a greater magnitude than the current I_2 as depicted in Figure 3.

Because of this current magnitude difference, the sinusoidal voltage wave 302 will shift downward to form a shifted sinusoidal voltage wave 302'. At this point, it should be evident that the shifted sinusoidal voltage wave 302' will be positive for a shorter amount of time T_1 than it is negative T_2. However, over a full cycle, the current flowing in one direction (i.e., I_1) across the plasma has to be the same as the current flowing in the other direction (i.e., I_2). Figure 4B illustrates how a total current during time T_1 for the larger magnitude current I_1 will actually equal a total current during a time T_2 for a smaller magnitude current I_2. Specifically, the area under 320a defines the net current for I_1 and the area under 320b defines the net current for I_2. For reference purposes only, the net current under area 310a and 310b are also equal to each other in a non-shifted system.

Referring back to Figure 4A, a wave portion 306 is the result of a half-wave rectification that is induced by the generated plasma. When a time average is taken over one cycle of the wave portion 306, a bias voltage on the surface of the top electrode is produced. In a like manner, a wave portion 308 is the result of another half-wave rectification that was induced by the generated plasma. Upon taking a time average over one cycle of the wave portion 308, a bias voltage on the surface of the

wafer is produced. It is important to note that the bias voltage produced on the surface of the wafer 206 has substantially increased over the standard bias voltage. That is, in prior art systems, the applied bias voltage is generally equally applied to both the surface of the top electrode and the surface of the wafer. Thus, by increasing the surface area of the sheath 231 that is proximate to the top electrode 200 surface, it is possible to increase the bias voltage over the surface of wafer 206, while slightly decreasing the bias voltage over the surface of the top electrode 200.

Figure 5 shows a graph illustrating bias vs. area ratio for the plasma sheaths of the top electrode 200 and the wafer 206, assuming that a sinusoidal RF potential is used and proper current balancing is in effect, in accordance with one embodiment of the present invention. When the sheath areas of the top electrode 200 and wafer 206 are about the same, the bias voltage (i.e., Electrode Potential/Vpeak) on both the top electrode 200 and wafer 206 will be about -0.3. However, the bias voltage of the top electrode 200 is shown to decrease as the area ratio increases. Conversely, the bias of the wafer 206 is shown to increase as the area ratio increases.

In a preferred embodiment, when the plasma sheath 231 has an $area_1$ that is about 2.7 times greater than the $area_2$ of the plasma sheath 232, the bias voltage on the wafer 206 will increase to about -0.75, while the bias voltage on the top electrode 200 will decrease to about -0.05. Because the bias voltage is now greater on the surface of the wafer 206, a larger ion bombardment energy will be present on the surface of the wafer 206 to assist in high aspect ratio semiconductor etching operations.

As an advantage, it is now possible to increase the bias voltage over the surface of the wafer 206 without causing an increase in plasma density. As mentioned above, when the plasma density is caused to increase beyond an acceptable

level, the processing gases may fail to perform their desired etching functions. Further yet, because an increased bias voltage is essentially an increase in ion bombardment energy, higher aspect ratio geometries can now be etched without causing premature etch stops, bow etch effects, or process window shifts.

In addition, although the above described parameters are associated with chambers configured to process "8 inch wafers," the parameters may be modified for application to substrates of varying sizes and shapes, such as those employed in the manufacture of semiconductor devices and flat panel displays. While this invention has been described in terms of several preferred embodiments, there are alterations, permutations, and equivalents which fall within the scope of this invention. It should also be noted that there are many alternative ways of implementing the methods and apparatuses of the present invention. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and equivalents as fall within the true spirit and scope of the present invention.

What is claimed is:

Claims

1. In a system for processing a semiconductor wafer through plasma etching operations, the system including a process chamber having a support chuck for holding the semiconductor wafer and a pair of RF power sources; the system comprising:

an electrode being positioned within the system and over the semiconductor wafer, the electrode having a center region, a first surface and a second surface, the first surface is configured to receive processing gases from a source that is external to the system and flow the processing gases into the center region, the second surface has a plurality of gas feed holes that are continuously coupled to a corresponding plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings are configured to define an electrode surface that is defined over a wafer surface of the semiconductor wafer.

2. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 1, wherein the electrode is coupled to one of the pair of RF power sources and the support chuck is coupled to the other one of the pair of RF power sources.

3. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 2, wherein a plasma is defined between the second surface of the electrode and the wafer surface.

4. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 3, wherein a first plasma sheath is defined next to the wafer surface and a second plasma sheath is defined next to the second surface, and the second plasma sheath follows an outline defined by the electrode openings of the second surface of the electrode.

5. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 4, wherein the first plasma sheath has a first area and the second plasma sheath has a second area, and the second area of the second plasma sheath is larger than the first area of the second plasma sheath.

6. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 1, wherein the electrode openings are at least about 5 mm or greater in diameter and the gas feed holes have a diameter of about 1 mm.

7. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 6, wherein a separation of between about 0.75 cm and about 4 cm is defined between the electrode surface and the wafer surface.

8. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 1, wherein two or more gas buffer plates are contained within the center region of the electrode.

9. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 1, wherein the electrode openings are defined in a hexagonal pattern arrangement throughout the second surface of the electrode.

10. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 5, wherein the second area of the second plasma sheath is between about 2 and 3 times greater than the first area of the first plasma.

11. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 10, wherein the second area of the second plasma sheath is about 2.7 times greater than the first area of the first plasma sheath.

12. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 10, wherein when the second area of the second plasma sheath is greater than the first area of the first plasma sheath, an increase in bias voltage is applied to the wafer surface and a decrease in bias voltage is applied to the second surface of the electrode.

13. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 12, wherein the increase in bias voltage causes an increase in ion bombardment energy onto the wafer surface, thereby increasing etch control.

14. In a chamber for processing a semiconductor wafer through plasma etching operations, the chamber including a support chuck for holding the semiconductor wafer and a pair of RF power sources; a method for making a top electrode for the chamber, comprising:

forming the top electrode to have a center region, a first surface and a second surface, the first surface has an inlet that is configured to receive processing gases from a source that is external to the system and flow the processing gases into the center region, the second surface has a plurality of gas feed holes that lead to a plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings are configured to define an electrode surface that is defined over a wafer surface of the semiconductor wafer.

15. The method for making a top electrode for the chamber as recited in claim 14, further comprising:

coupling the top electrode to one of the pair of RF power sources and the support chuck to the other one of the pair of RF power sources.

16. The method for making a top electrode for the chamber as recited in claim 15, further comprising:

forming the electrode openings to be at least about 5 mm or greater in diameter and the gas feed holes to have a diameter of about 1 mm.

17. The method for making a top electrode for the chamber as recited in claim 15, further comprising:

defining the electrode openings to a depth of between about 1/32 inch and ¼ inch.

18. The method for making a top electrode for the chamber as recited in claim 16, further comprising:

fixing a separation of between about 0.75 cm and about 4 cm between the electrode surface and the wafer surface.

19. The method for making a top electrode for the chamber as recited in claim 18, further comprising:

inserting two or more gas buffer plates within the center region of the top electrode.

20. The method for making a top electrode for the chamber as recited in claim 18, further comprising:

striking a plasma between the separation, the plasma having a first plasma sheath that is proximate to the wafer surface and a second plasma sheath that outlines an inner region of the top electrode openings, such that the second plasma sheath has an area that is greater than the first plasma sheath.

21. The method for making a top electrode for the chamber as recited in claim 20, further comprising:

increasing an ion bombardment energy over the wafer surface when the second plasma sheath has the area that is greater than the first plasma sheath.

22. A plasma process chamber for processing a semiconductor wafer, the plasma process chamber including a support chuck for holding the semiconductor wafer and a pair of RF power sources, the plasma process chamber, comprising:

an electrode means for providing gas chemistries into a process region that is defined between the electrode means and a wafer surface of the semiconductor wafer, the electrode means having a plurality of oversized gas feed holes that are configured to define an electrode surface over the wafer surface; and

wherein when a plasma is generated between the electrode surface and the wafer surface in the plasma process chamber, a substantially planar first plasma sheath is defined over the wafer surface and a contoured second plasma sheath is defined over the electrode surface, such that the contoured second plasma sheath

extends into the plurality of oversized gas feed holes, and therefore the contoured second plasma sheath has a greater surface area than the substantially planar first plasma sheath.

23. A plasma process chamber for processing a semiconductor wafer as recited in claim 22, wherein the oversized gas feed holes are arranged in a hexagonal pattern throughout the electrode surface.

24. A plasma process chamber for processing a semiconductor wafer as recited in claim 23, wherein each of the oversized gas feed holes have a diameter that is set to be about 5 mm or greater.

25. A plasma process chamber for processing a semiconductor wafer as recited in claim 22, wherein when the contoured second plasma sheath has a greater surface area than the substantially planar first plasma sheath, an increased bias voltage is generated over the wafer surface and a decreased bias voltage is generated over the electrode surface.

26. A plasma process chamber for processing a semiconductor wafer as recited in claim 25, wherein the increase in bias voltage over the wafer surface causes in increase in ion bombardment energy over the wafer surface and an increase in etch control of high aspect ratio features.

27. In a system for processing a semiconductor wafer through plasma etching operations, the system including a process chamber having a support chuck for supporting the semiconductor wafer and having a RF power source connected thereto; the system comprising:

a grounded electrode being positioned within the system and over the semiconductor wafer, the grounded electrode having a center region, a first surface and a second surface, the first surface is configured to receive processing gases from a source that is external to the system and flow the processing gases into the center region, the second surface has a plurality of gas feed holes that are continuously coupled to a corresponding plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes, the plurality of electrode openings are configured to define an electrode surface that is defined over a wafer surface of the semiconductor wafer.

28. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 27, wherein a plasma is defined between the second surface of the electrode and the wafer surface.

29. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 28, wherein a first plasma sheath is defined next to the wafer surface and a second plasma sheath is defined next to the second surface,

and the second plasma sheath follows an outline defined by the electrode openings of the second surface of the electrode.

30. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 29, wherein the first plasma sheath has a first area and the second plasma sheath has a second area, and the second area of the second plasma sheath is larger than the first area of the second plasma sheath.

31. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 27, wherein the electrode openings are at least about 5 mm or greater in diameter and the gas feed holes have a diameter of about 1 mm.

32. The system for processing a semiconductor wafer through plasma etching operations as recited in claim 30, wherein when the second area of the second plasma sheath is greater than the first area of the first plasma sheath, an increase in bias voltage is applied to the wafer surface and a decrease in bias voltage is applied to the second surface of the electrode.

SEMICONDUCTOR PROCESS CHAMBER ELECTRODE AND METHOD FOR MAKING THE SAME

ABSTRACT OF THE DISCLOSURE

Disclosed is a system for processing a semiconductor wafer through plasma etching operations. The system has a process chamber that includes a support chuck for holding the semiconductor wafer and a pair of RF power sources. In another case, the system can be configured such that the electrode is grounded and the pair of RF frequencies are fed to the support chuck (bottom electrode). The system therefore includes an electrode that is positioned within the system and over the semiconductor wafer. The electrode has a center region, a first surface and a second surface. The first surface is configured to receive processing gases from a source that is external to the system and flow the processing gases into the center region. The second surface has a plurality of gas feed holes that are continuously coupled to a corresponding plurality of electrode openings that have electrode opening diameters that are greater than gas feed hole diameters of the plurality of gas feed holes. The plurality of electrode openings are configured to define an electrode surface that is defined over a wafer surface of the semiconductor wafer. The electrode surface assists in increasing an electrode plasma sheath area in order to cause a shift in bias voltage onto the wafer surface, thereby increasing the ion bombardment energy over the wafer without increasing the plasma density.

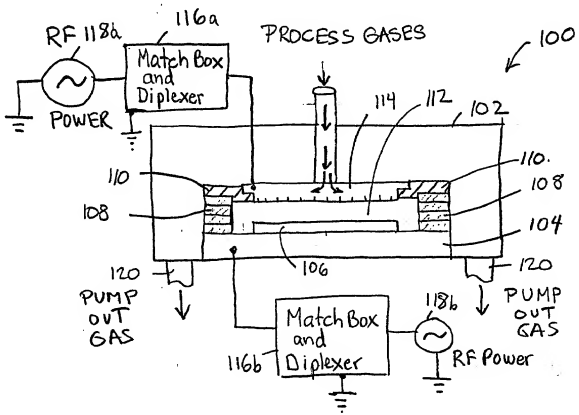


FIG. 1A
(prior art)

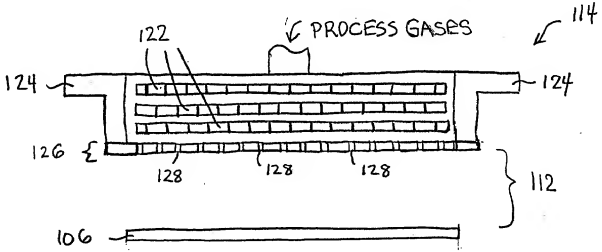


FIG. 1B
(prior art)

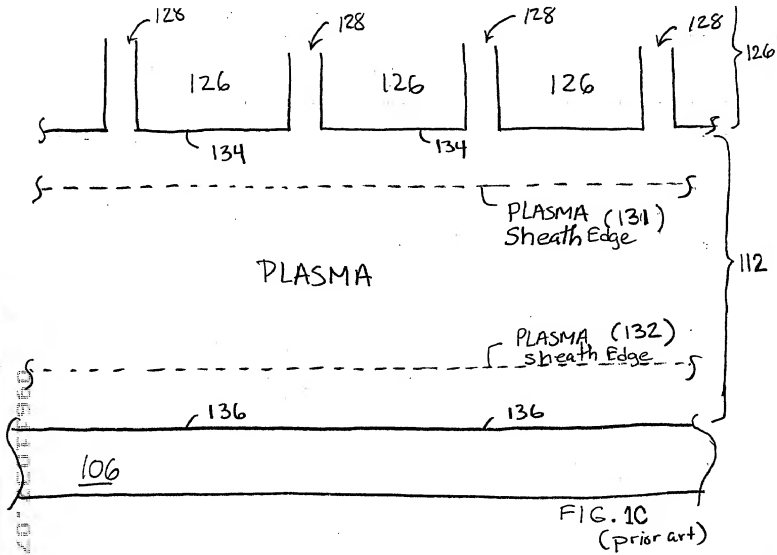


FIG. 1C
(prior art)

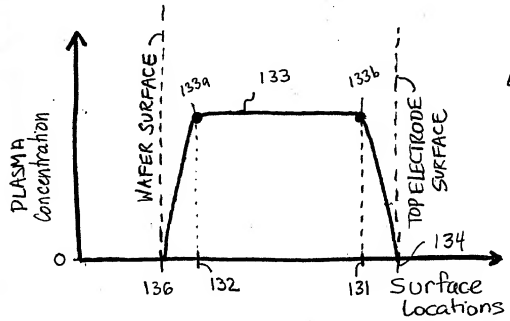


FIG. 1D
(prior art)

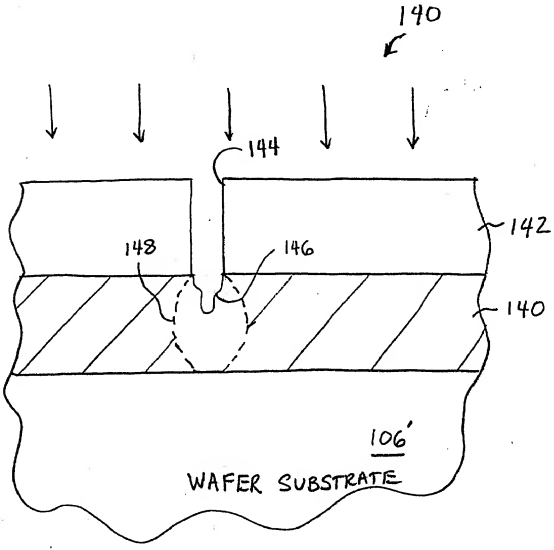


FIG. 1E
(prior art)

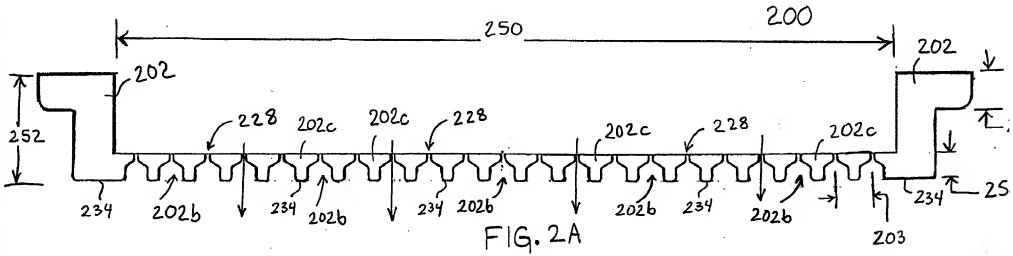


FIG. 2A

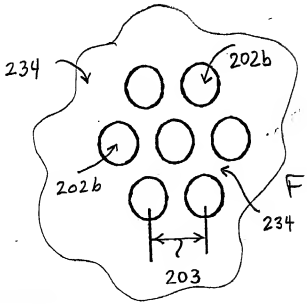
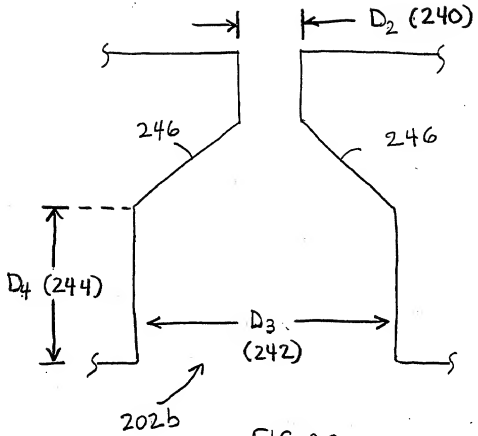


FIG. 2B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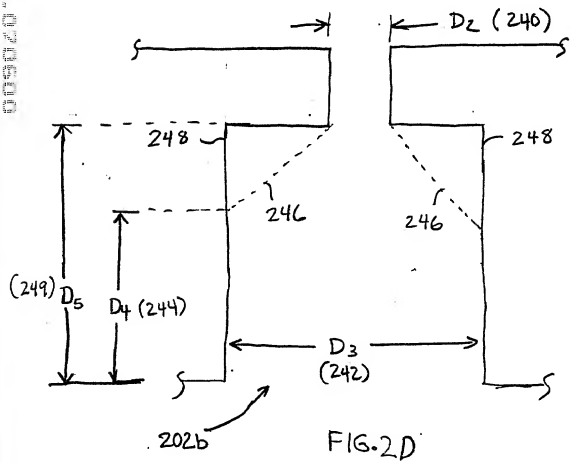
246
D4 (244)
D3
(242)
202b

FIG. 2C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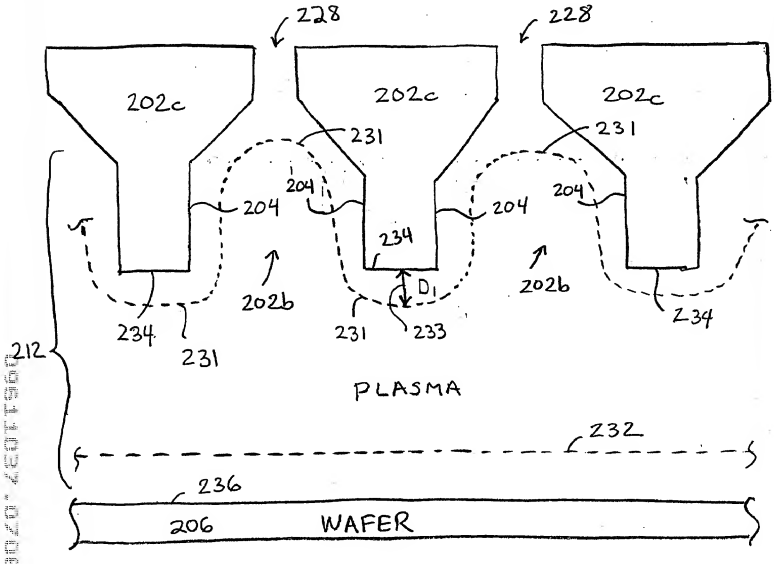
248
248
246
246
(249) D5
D4 (244)
D3
(242)
202b

FIG. 2D


228
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202c
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204
204
234
202b
202b
234
231
231
233
234
D1
212
PLASMA
232
236
206
WAFER

FIG. 2E

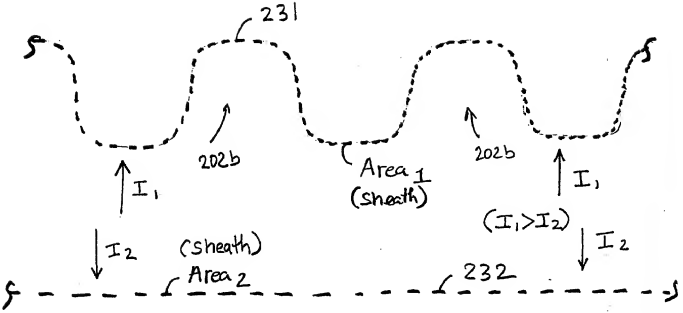

FIG. 3

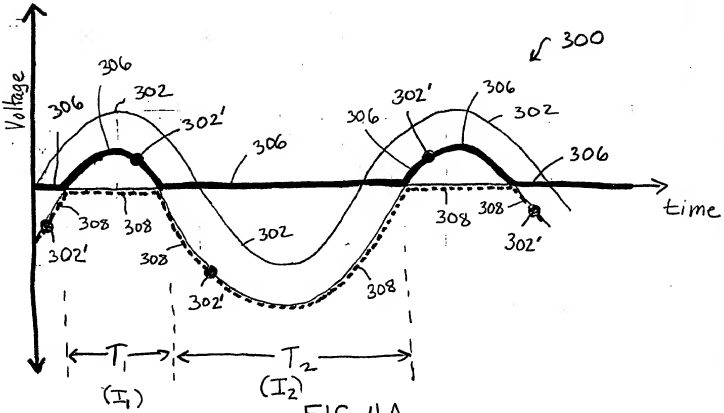

FIG. 4A

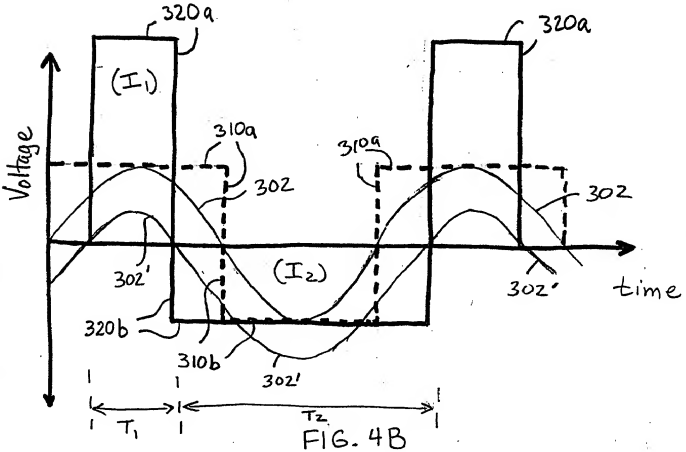
320a
320a
(I1)
310a
310a
302
302
Voltage
302'
(I2)
302'
time
320b
310b
302'
T1
T2

FIG. 4B

Bias vs. Area Ratio

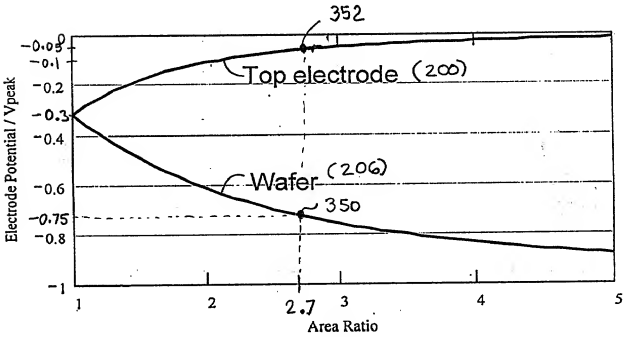

FIG. 5

DECLARATION AND POWER OF ATTORNEY FOR ORIGINAL U.S. PATENT APPLICATION

Attorney's Docket No. LAM1P077

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: SEMICONDUCTOR PROCESS CHAMBER ELECTRODE AND METHOD FOR MAKING THE SAME, the specification of which,

(check one)

1. ☒ is attached hereto.

2. ☐ was filed on _____ as U.S. Application Serial No. _____ and was amended on _____.

3. ☐ was filed on _____ as International PCT Application Serial No. _____ and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, CFR § 1.56.

I hereby claim foreign priority benefits under Title 35, United States code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Benefits Claimed?
_____ (Appl. No.)	_____ (Country)	_____ (Filing Date)	☐Yes ☐No
_____ (Appl. No.)	_____ (Country)	_____ (Filing Date)	☐Yes ☐No
_____ (Appl. No.)	_____ (Country)	_____ (Filing Date)	☐Yes ☐No

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below:

_____ (Application Serial No.)	_____ (Filing Date)
_____ (Application Serial No.)	_____ (Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Application(s)

(Application Serial No.)	(Filing Date)	(Status - patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status - patented, pending, abandoned)

And I hereby appoint the law firm of Hickman & Martine, LLP, including **Paul L. Hickman (Reg. No. 28, 516); Albert S. Penilla (Reg. No. 39,487); Brian R. Coleman (Reg. No. 39,145); Peter B. Martine (Reg. No. 32,043); Dawn L. Palmer (Reg. No. 41,238); Raymis H. Kim (Reg. No. 39,462); and Jerray Wei (Reg. No. 43,247)** as my principal attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

Send Correspondence To:

Albert S. Penilla
HICKMAN & MARTINE, LLP
P.O. BOX 52037
Palo Alto, California 94306

Direct Telephone Calls To: **Albert S. Penilla at telephone number (650) 470-7430**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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Inventor's signature: [signature] — **Date of Signature:** 6/18/98

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Inventor's signature: [signature] — **Date of Signature:** 6/18/98

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